

5 WHAT IS CLAIMED IS:

1. A semiconductor component comprising:  
a base die comprising a substrate having a back side,  
and a plurality of conductive vias in the substrate;  
10 a secondary die having a circuit side bonded to the  
back side and a plurality of contacts bonded to the  
conductive vias; and  
a plurality of terminal contacts on the base die in  
electrical communication with the conductive vias.  
15
2. The semiconductor component of claim 1 further  
comprising an encapsulant on the back side at least  
partially encapsulating the secondary die.
- 20 3. The semiconductor component of claim 1 further  
comprising a polymer layer on the base die configured as a  
protective member, a rigidifying member and a stencil for  
forming the terminal contacts.
- 25 4. The semiconductor component of claim 1 further  
comprising a second secondary die bonded to the secondary  
die.
5. The semiconductor component of claim 1 the base  
30 die and the secondary die comprise thinned dice.
6. The semiconductor component of claim 1 wherein the  
conductive vias comprise openings in the substrate at least  
partially filled with a conductive material.  
35
7. A semiconductor component comprising:  
a thinned base die comprising a circuit side, a back  
side, a plurality of conductive vias and a plurality of

5 contacts on the back side in electrical communication with  
the conductive vias;

a thinned secondary die stacked on the base die and  
bonded to the contacts; and

10 a plurality of terminal contacts on the circuit side  
in electrical communication with the conductive vias.

8. The semiconductor component of claim 7 further  
comprising an encapsulant on the back side at least  
partially encapsulating the secondary die.

15

9. The semiconductor component of claim 7 further  
comprising a cap plate bonded to the secondary die  
comprising a plurality of conductors configured to  
electrically connect selected base die contacts to selected  
20 secondary die contacts.

10. The semiconductor component of claim 7 further  
comprising a cap plate bonded to the secondary die and a  
plurality of electrical components on the cap plate in  
25 electrical communication with the secondary die.

11. The semiconductor component of claim 7 wherein  
the contacts comprise bumps in physical contact with the  
conductive vias.

30

12. The semiconductor component of claim 7 wherein a  
peripheral outline of the base die matches that of the  
component.

35 13. The semiconductor component of claim 7 wherein  
the conductive vias comprise a metal and a solder alloy.

14. A semiconductor component comprising:

5        a base die comprising a thinned semiconductor  
substrate and a plurality of conductors on the substrate;  
an internal signal transmission system comprising a  
plurality of conductive vias in the substrate in electrical  
communication with the conductors, and a plurality of  
10    contacts on the conductive vias;  
a secondary die bonded to the contacts; and  
a plurality of terminal contacts on the conductors.

15        15. The semiconductor component of claim 14 wherein  
the secondary die comprises a plurality of metal bumps  
bonded to the contacts.

20        16. The semiconductor component of claim 14 wherein  
the conductors comprise redistribution conductors on a  
circuit side of the base die.

25        17. The semiconductor component of claim 14 further  
comprising a cap plate bonded to the secondary die and a  
plurality of electrical components on the cap plate in  
electrical communication with the secondary die.

30        18. The semiconductor component of claim 14 further  
comprising a cap plate bonded to the secondary die  
configured to short selected contacts on the base die to  
selected contacts on the secondary die.

35        19. The semiconductor component of claim 14 further  
comprising an electrically conductive polymer bonding the  
secondary die to the contacts.

20. The semiconductor component of claim 14 further  
comprising a module substrate bonded to the base die.

5           21. The semiconductor component of claim 14 wherein  
the secondary die and the substrate have a thickness of  
about 100  $\mu\text{m}$  to 600  $\mu\text{m}$ .

10           22. The semiconductor component of claim 14 wherein  
the conductive vias comprise openings in the substrate at  
least partially filled with a material selected from the  
group consisting of metal, solder, conductive polymers and  
nano-particle conductive polymers.

15           23. A semiconductor component comprising:  
a base die comprising a thinned semiconductor  
substrate having a peripheral outline, a circuit side, a  
back side, and a plurality of conductive vias in the  
substrate;

20           a thinned secondary die bonded to the back side and  
comprising a plurality of integrated circuits in electrical  
communication with the conductive vias;

an encapsulant on the back side having the peripheral  
outline and at least partially encapsulating the secondary  
25 die;

a polymer layer on the circuit side having the  
peripheral outline and configured as a protective and  
rigidifying member for the component; and

30           a plurality of terminal contacts on the circuit side  
in electrical communication with the conductive vias.

24. The semiconductor component of claim 23 wherein  
the polymer layer is configured as a stencil for forming  
the terminal contacts.

35           25. The semiconductor component of claim 23 wherein  
the secondary die comprises a plurality of bumped contacts  
bonded to the conductive vias.

5           26. The semiconductor component of claim 23 wherein  
the base die comprises a plurality of bumped contacts on  
the conductive vias bonded to the secondary die.

10           27. The semiconductor component of claim 23 further  
comprising a second secondary die bonded to the thinned  
secondary die in electrical communication with the  
conductive vias.

15           28. A semiconductor component comprising:  
a first base die comprising a plurality of first  
conductive vias;  
a second base die stacked and bonded to the first base  
die comprising a plurality of second conductive vias in  
electrical communication with the first conductive vias;  
20           a secondary die stacked and bonded to the second base  
die comprising a plurality of bumped contacts bonded to the  
second conductive vias; and  
a plurality of terminal contacts on the first base die  
in electrical communication with the first conductive vias.

25           29. The semiconductor component of claim 28 wherein  
the terminal contacts comprise balls or bumps in a grid  
array.

30           30. The semiconductor component of claim 28 further  
comprising an underfill layer between the first base die  
and the secondary die.

35           31. The semiconductor component of claim 28 wherein  
the first base die, the second base die and the secondary  
die comprise known good dice.

5           32. The semiconductor component of claim 28 wherein  
the secondary die comprises a cap plate having a plurality  
of electrical components thereon.

10           33. The semiconductor component of claim 28 wherein  
the first conductive vias and the second conductive vias  
comprise a material selected from the group consisting of  
metal, solder, conductive polymers and nano-particle  
conductive polymers.

15           34. The semiconductor component of claim 28 wherein  
the bumped contacts comprise metal bumps in physical  
contact with the conductive vias.

20           35. A semiconductor component comprising:

a base die comprising a semiconductor substrate having  
a circuit side and a back side, a plurality of die contacts  
on the circuit side, a plurality of conductive vias in the  
substrate in electrical communication with the die  
contacts, a plurality of redistribution conductors on the  
25 circuit side in electrical communication with the  
conductive vias, and a plurality of terminal contacts on  
the circuit side in electrical communication with the  
conductors;

a secondary die bonded to the back side;

30 an underfill layer bonding the secondary die to the  
base die; and

a plurality of bumped contacts bonded to the  
conductive vias and to the secondary die.

35           36. The semiconductor component of claim 35 further  
comprising a polymer layer on the circuit side configured  
as a rigidifying member, a protective member, and a stencil  
for forming the terminal contacts.

5           37. The semiconductor component of claim 35 further comprising a module substrate bonded to the base die.

          38. The semiconductor component of claim 35 further comprising an encapsulant on the back side at least  
10 partially encapsulating the secondary die.

          39. The semiconductor component of claim 35 further comprising an electrically insulating polymer layer in the conductive vias and on the back side.  
15

          40. The semiconductor component of claim 35 wherein the base die and the secondary die comprise thinned dice.

          41. The semiconductor component of claim 35 wherein  
20 the terminal contacts comprise bumps, balls or pins in a grid array.

          42. The semiconductor component of claim 35 wherein the conductive vias comprise lasered openings and a  
25 conductive material in the openings, and the bumped contacts comprise solder bumps bonded to the conductive material.

          43. The semiconductor component of claim 35 wherein  
30 the base die and the component have a same peripheral outline.

          44. The semiconductor component of claim 35 wherein the conductive vias comprise openings in the substrate, an  
35 insulating layer on the openings, and a conductive material in the openings.

          45. A semiconductor component comprising:

5 a base die comprising a circuit side, a back side, a plurality of conductive vias and a plurality of contacts on the back side in electrical communication with the conductive vias;

10 a first secondary die stacked on the base die and bonded to the contacts, the first secondary die comprising a plurality of secondary conductive vias and a plurality of secondary contacts in electrical communication with the secondary conductive vias;

15 a second secondary die stacked on the first secondary die and bonded to the secondary contacts; and

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

20 46. The semiconductor component of claim 45 further comprising an encapsulant on the back side at least partially encapsulating the first secondary die and the second secondary die.

25 47. The semiconductor component of claim 45 further comprising a polymer layer on the circuit side configured as a rigidifying member, a protective member, and a stencil for forming the terminal contacts.

30 48. The semiconductor component of claim 45 wherein the base die, the first secondary die and the second secondary die comprise thinned dice.

35 49. The semiconductor component of claim 45 wherein the second secondary die includes a plurality of electrical components thereon in electrical communication with the secondary contacts.



5           50. The semiconductor component of claim 45 wherein  
the contacts comprise bumps in physical contact with the  
conductive vias.

10           51. A method for fabricating a semiconductor  
component comprising:

          providing a base die comprising a substrate having a  
back side;

          forming a plurality of conductive vias in the  
substrate;

15           providing a secondary die comprising a circuit side  
and a plurality of contacts;

          bonding the secondary die to the back side and the  
contacts to the conductive vias; and

20           forming a plurality of terminal contacts on the base  
die in electrical communication with the conductive vias.

          52. The method of claim 51 further comprising prior  
to the bonding step thinning the base die, and following  
the bonding step thinning the secondary die.

25

          53. The method of claim 51 further comprising forming  
a polymer layer on the base die proximate to the terminal  
contacts configured to protect and rigidify the component.

30           54. The method of claim 51 wherein the forming the  
conductive vias step comprises laser machining openings  
from the back side into the substrate, forming insulating  
layers in the openings and depositing a conductive material  
in the openings.

35

          55. The method of claim 51 wherein the forming the  
conductive vias step comprises forming openings in the  
substrate depositing a metal in the openings and then  
squeegeeing a solder into the openings.

5

56. A method for fabricating a semiconductor component comprising:

providing a base die comprising a circuit side, a back side, a semiconductor substrate and a plurality of  
10 conductive vias in the substrate;

providing a secondary die comprising a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias; and

15 forming a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

57. The method of claim 56 further comprising forming  
20 an encapsulant on the back side at least partially encapsulating the secondary die.

58. The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base  
25 dice and the bonding step is performed by placing a plurality of secondary dice on the base dice.

59. The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base  
30 dice, the secondary die is contained on a secondary wafer containing a plurality of secondary dice and the bonding step is performed by bonding the base wafer to the secondary wafer.

35 60. The method of claim 56 further comprising forming a polymer layer on the circuit side configured as a stencil for forming the terminal contacts.

5           61. The method of claim 56 wherein the base die and the secondary die comprise thinned dice.

          62. A method for fabricating a semiconductor component comprising:

10           providing base die on a base wafer;  
          forming a plurality of conductive vias on the base die;

          providing a secondary die comprising a plurality of contacts;

15           bonding the secondary die to the base die with the contacts in electrical communication with the conductive vias;

          thinning the secondary die while bonded to the base die on the wafer;

20           forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias; and

          singulating the base die with the secondary die bonded thereto from the wafer.

25

          63. The method of claim 62 further comprising thinning the base die on the base wafer prior to the bonding step.

30           64. The method of claim 62 wherein the forming the conductive vias step comprises forming openings in the base die and at least partially filling the openings with a metal a conductive polymer, or a nano particle conductive polymer.

35

          65. The of claim 62 further comprising testing the secondary die and the base die prior to the bonding step.

5           66.     The method of claim 62 further comprising  
following the singulating step mounting the base die to a  
module substrate.

10           67.     The method of claim 62 wherein the secondary die  
is contained on a secondary wafer and the bonding step is  
performed by bonding the secondary wafer to the base wafer.

            68.     A method for fabricating a semiconductor  
component comprising:

15           providing a tested singulated secondary die comprising  
a plurality of bumped contacts;

            providing a wafer comprising a base die comprising a  
substrate having a circuit side and a back side, a  
plurality of integrated circuits in the substrate, and a  
20           plurality of contacts on the substrate in electrical  
communication with the integrated circuits;

            forming a polymer layer on the circuit side having  
openings aligned with the contacts;

25           forming a plurality of conductive vias in the back  
side extending through the substrate to the contacts;

            bonding the secondary die to the back side with the  
bumped contacts in electrical communication with the  
conductive vias; and

30           forming terminal contacts in the openings using the  
polymer layer as a stencil.

            69.     The method of claim 68 wherein the forming the  
polymer layer step is performed using a laser imaging  
process.

35

            70.     The method of claim 68 wherein the laser imaging  
process comprises heat curing or UV curing the polymer  
layer.

5        71. The method of claim 68 wherein the forming the polymer layer step comprises depositing and curing a polymer material.

10       72. The method of claim 68 wherein the forming the polymer layer step is performed using a photo lithography process.

15       73. The method of claim 68 wherein the forming the conductive vias step comprises laser machining and thinning the base die.

20       74. The method of claim 68 further comprising following the bonding step, thinning the secondary die by grinding, polishing, or etching the secondary die.

25       75. A method for fabricating a semiconductor component comprising:

      providing a base die comprising a substrate having a back side;

      forming a plurality of conductive vias in the substrate;

      providing a first secondary die comprising a circuit side, a plurality of contacts and a plurality of secondary conductive vias;

30       bonding the secondary die to the back side and the contacts to the conductive vias;

      providing a second secondary die; and

      bonding the second secondary die to the first secondary die in electrical communication with the secondary conductive vias.

35       76. The method of claim 75 further comprising forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

5

77. The method of claim 75 further comprising thinning the first secondary die, the second secondary die and the base die.

10

78. The method of claim 75 wherein the forming the conductive vias step comprises laser machining openings in the substrate and then depositing a nano particle conductive polymer in the openings.

15

79. The method of claim 75 further comprising forming a polymer layer on the base die configured to protect and rigidify the component.

80. A system comprising:

20

a substrate; and

25

a semiconductor component on the substrate comprising a base die comprising a substrate having a back side, and a plurality of conductive vias in the substrate, a secondary die having a circuit side bonded to the back side and a plurality of contacts bonded to the conductive vias, and a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

30

81. The system of claim 80 further comprising a cap plate bonded to the secondary die configured to short selected contacts on the base die to selected contacts on the secondary die.

35

81. The system of claim 80 further comprising a cap plate bonded to the secondary die and at least one electrical element on the cap plate in electrical communication with the secondary die.

5

83. The system of claim 80 wherein the substrate is contained in a device selected from the group consisting of a module, a package, a computer, a camcorder, a camera, a cell phone, and a medical device.

10

84. The system of claim 80 further comprising an encapsulant on the back side at least partially encapsulating the secondary die.

15

85. The system of claim 80 further comprising a polymer layer on the base die configured as a protective member, a rigidifying member and a stencil for forming the terminal contacts.

20

86. A system comprising:

a substrate comprising a plurality of electrodes; and  
a semiconductor component on the substrate comprising:

25

a thinned base die comprising a circuit side, a back side, a plurality of conductive vias and a plurality of contacts on the back side in electrical communication with the conductive vias;

a thinned secondary die stacked on the base die and bonded to the contacts; and

30

a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias and bonded to the electrodes.

35

87. The system of claim 86 further comprising a second secondary die stacked on and bonded to the secondary die.

5           88. The system of claim 86 further comprising a cap  
plate stacked on and bonded to the secondary die.

          89. The system of claim 86 wherein the system  
comprises a multi chip module, a system in a package, a  
10 computer, a camcorder, a camera, a cell phone, or a medical  
device.

          90. A system comprising:  
a substrate comprising a plurality of electrodes;  
15 a semiconductor component on the substrate comprising:  
a base die comprising a thinned substrate having  
a peripheral outline and a plurality of conductive  
vias in the substrate;  
a thinned secondary die comprising a plurality of  
20 bumped contacts bonded to the conductive vias and  
electrically connecting the base die and the secondary  
die;  
an encapsulant on the base die having the  
peripheral outline and at least partially  
25 encapsulating the secondary die;  
a rigidifying polymer layer on the base die  
having the peripheral outline; and  
a plurality of terminal contacts on the base die  
proximate to the polymer layer in electrical  
30 communication with the conductive vias and bonded to  
the electrodes.

          91. The system of claim 90 wherein the substrate  
comprises a module substrate or a package substrate.  
35

          92. The system of claim 90 wherein the conductive  
vias comprise a material selected from the group consisting



5 of metal, solder, conductive polymers and nano particle  
conductive polymers.

93. The system of claim 90 further comprising a  
plurality of components on the substrate substantially  
10 identical to the component.

94. The system of claim 90 wherein the polymer layer  
comprises a stencil for forming the terminal contacts.

15 95. The system of claim 90 wherein the conductive  
vias comprise openings in the substrate, an insulating  
layer on the openings, and a conductive material in the  
openings.

20 96. The system of claim 90 further comprising a  
second secondary die stacked on and bonded to the secondary  
die.

97. The system of claim 90 further comprising a cap  
25 plate stacked on and bonded to the secondary die.

98. The system of claim 90 further comprising a cap  
plate stacked on and bonded to the secondary die and  
configured to short selected contacts on the base die to  
30 selected contacts on the secondary die.

99. The system of claim 90 further comprising a cap  
plate stacked on and bonded to the secondary die and a  
plurality of electrical components on the cap plate in  
35 electrical communication with the secondary die.

5           100.    The system of claim 90 wherein the system  
          comprises a multi chip module, a system in a package, a  
          computer, a camcorder, a camera, a cell phone, or a medical  
          device.

10

15